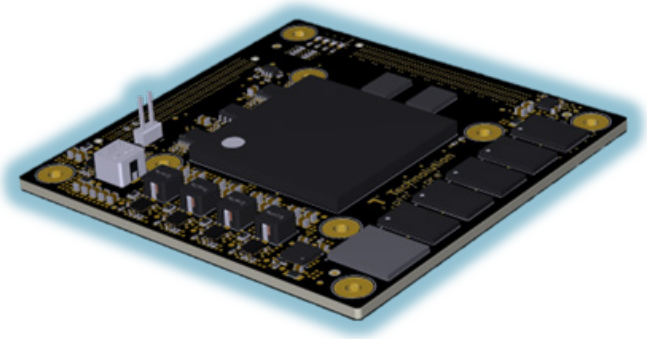
CDPU
Core Module



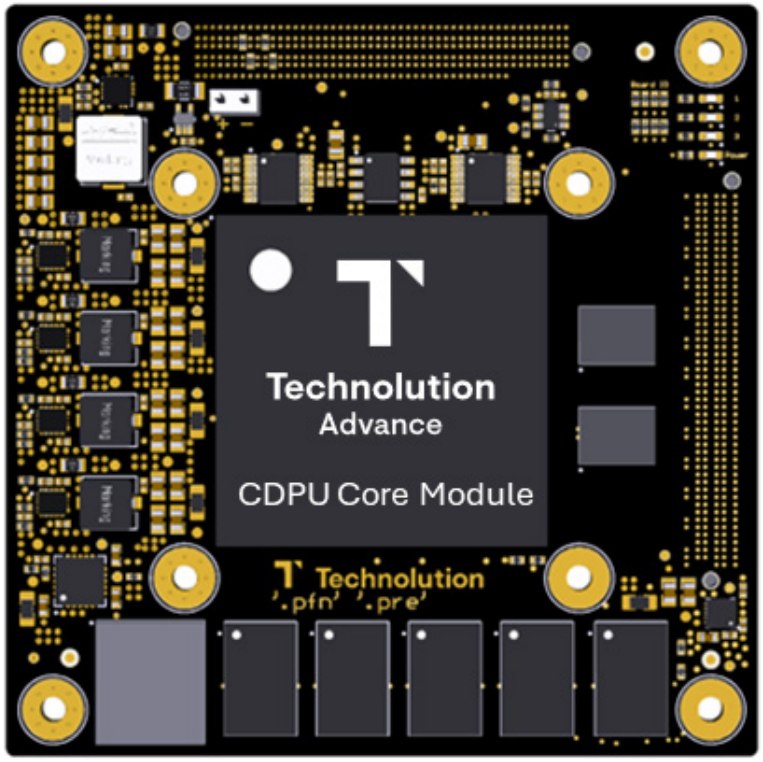
The CDPU Core Module is an 80 × 80 mm FPGA-SoC processing module based on the Microchip PolarFire SoC MPFS460T.

It combines 64-bit RISC-V processing, programmable logic, DDR4 memory and non-volatile storage on a compact board intended for integration on a mission-specific carrier.

The board-to-board interfaces provide access to high-speed transceivers, general-purpose and configurable I/O, enabling the carrier to implement the required payload and spacecraft interfaces.

Key architectural features

- Integrated 64-bit RISC-V quad core processor subsystem and FPGA fabric
- FPGA resources available for custom processing, protocol handling and hardware acceleration
- 4 GB DDR4 memory with ECC
- Onboard QSPI boot memory and eMMC storage
- High-speed serial and configurable I/O exposed through board-to-board connectors
- Carrier-based architecture for mission -specific interfaces and functionality
- Linux-based software environment



Core Module Specifications

Processor and FPGA

- Microchip PolarFire SoC MPFS460T
- 1 x 64-bit RV64IMAC monitor/boot core
- 4 x 64-bit RV64GC application core
- Fmax cores: 667 MHz
- Logic elements: 461k
- Math blocks: 1,420
- Fabric uProm: 553 kbit
- Total RAM: 31600 kbit
- PLLs: 8
- High-speed transceivers: up to 12.7 Gbit/s
- PCIe interface

Memory and storage

- 4GB DDR4 with EC
- 40GB eMMC Flash
- 64MB QSPI Flash

Board-to-board interfaces

- 12 × high-speed transceiver lanes
- 3 × transceiver reference clocks
- 106 × GPIO
- 84 × HSIO
- 28 × MSSIO
- 4 × ADC inputs

Electrical

- Single supply: 5 VDC

Software environment

- Linux / Yocto BSP
- Bare-metal development support
- RTOS support planned

Technolution B.V.
Burgemeester Jamessingel 1
2803 WV Gouda
The Netherlands

+31 (0)182 59 40 00
advance@technolution.com
Technolution Advance

technolution.com/cdpu

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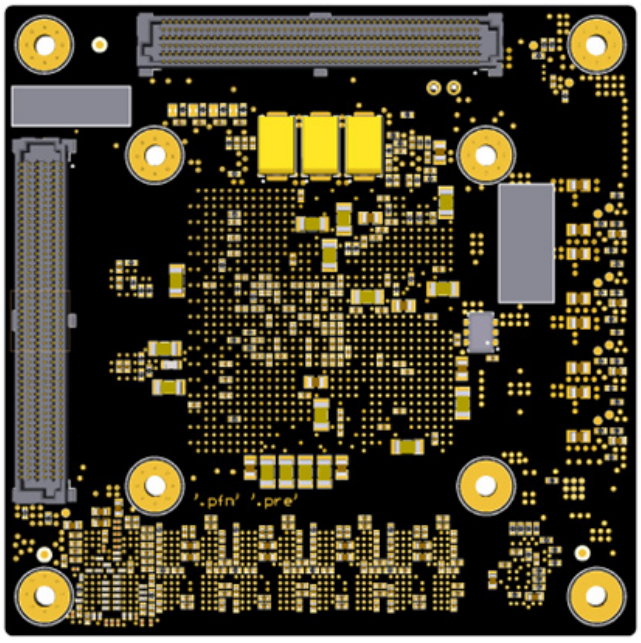


Software and logic development

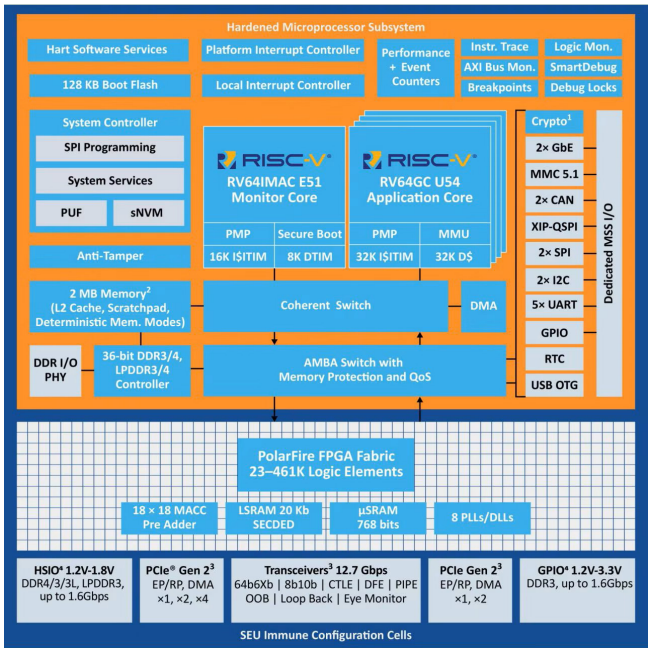
The CDPU Core Module supports software and FPGA development within a single FPGA-SoC architecture.

Software for the 64-bit RISC-V processor subsystem can be developed using standard RISC-V toolchains. A Linux distribution based on Yocto is provided as the baseline software environment. Bare-metal development is supported, with RTEMS support included on the product roadmap.

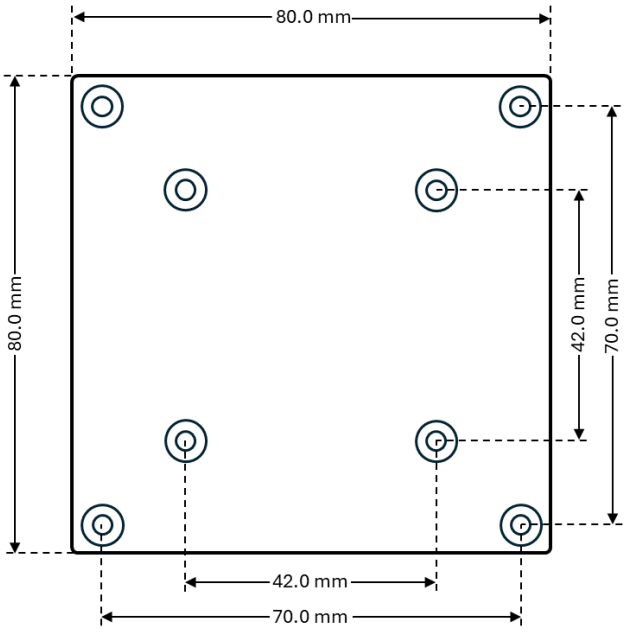
FPGA development, device configuration and hardware/software integration are performed using the Microchip Libero® SoC Design Suite.

The programmable logic can be used for application-specific processing, hardware acceleration, interface implementation and high-throughput data handling.

PolarFire SoC FPGA



Dimensions



Cooling